

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit: 2811 Examiner: Unassigned

In re PATENT APPLICATION of

Applicant: Teruhisa OBARA

Appl. No.: 10/649,765

Filed: August 28, 2003

For: SEMICONDUCTOR INTEGRATED

CIRCUIT WITH A TEST CIRCUIT

OUTPOUR STATEMENT

OUTPOUR STATEMENT

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

**OKI 368** 

Sir:

Atty. Dkt.:

This is an Information Disclosure Statement submitted in compliance with the timing requirements of 37 C.F.R. §1.97(b)(3), i.e., prior to a first Office Action on the merits.

Attached is a copy of a Japanese patent publication, which was cited in a Japanese Office Action dated March 30, 2004 that was issued by the Japanese Patent Office in connection with a Japanese counterpart application, together with the attached Englishlanguage translation and also an abstract. Since this Information Disclosure Statement is being filed before the first Office Action, no certification or fee is required, and the requirements of 37 C.F.R. §§1.97 and 1.98 are deemed to be fully met as to all documents listed. Consideration of the listed document is respectfully requested.

Should any fee be required, please charge the same to our Deposit Account No. 18-0002 and advise us accordingly.

Respectfully submitted,

July 22, 2004

Date

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CUSTOMER NO. 23995

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT				Atty Docket	Application	Application No.		
				OKI 368	10/649,765			
				Applicant	i			
				Teruhisa OBA	RA			
				Filing Date August 28, 2003	Group U 2811	Group Unit 2811		
				U.S. PATENT DOCUMENTS				
Examiner Initial		Document Number	Date	Name	Class	Sub- Class	Filing Date	
	AA							
	AB							
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	4		FO	REIGN PATENT DOCUMENTS	•			
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